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Patent

Customer No.: 31561
Docket No. 12409-US-PA
Application No.: 10/709,372

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Applicant	: Chang et al.
Application No.	: 10/709,372
Filed	: April 30, 2004
For	: NON-VOLATILE MEMORY CELL AND MANUFACTURING METHOD THEREOF
Art Unit	: 2818
Examiner	: TRAN, MAI HUONG C.

TRANSMITTAL LETTER
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Assistant Commissioner for Patent
Alexandria, VA 22314

In response to the Notice of Appeal filed on September 19, 2005, please find the *Appeal Brief* in 12 pages.

Please charge the payment in the amount of US$500 to account No. 50-2620 (Order No.: 12409-US-PA) to cover the fee set forth in 37 CFR 1.17(c) for filing an Appeal Brief.

If the payment is not fully covered in response thereof, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No.: 50-2620 (Order No.: 12409-US-PA).

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE CHANG et al.

Application for Patent

Filed April 30, 2004

Serial No. 10/709,372

FOR:

NON-VOLATILE MEMORY CELL AND MANUFACTURING METHOD THEREOF

(as amended)

APPEAL BRIEF

JIANQ CHYUN IP OFFICE
Attorneys for Applicants

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I. Real party in interest

The real party in interest is POWERCHIP SEMICONDUCTOR Corp., the assignee of record.

II. Related appeals and interferences

There are no related appeals and/or interferences.

III. Status of the claims

A total of 18 claims were presented during prosecution of this application. Claims 11-18 have been cancelled. Appellants appeal rejected claims 1-10.

IV. Status of amendments

A proposed amendment was filed by appellants on January 7th, 2005, proposing amendments to the claims by canceling claims 11-18 in response to the Restriction Requirement dated on December 20th, 2004. Another proposed amendment was filed by appellants on May 4th, 2005, proposing amendments to the claims in response to the first Office Action dated on February 4th, 2005. In the Final Office Action dated May 20th, 2005, the proposed amendment filed on May 4th, 2005 was entered. In response to the Final Office Action dated May 20th, 2005, a telephone interview was held with the Examiner on July 11th, 2005 and the appellants filed a response on August 18th, 2005 without further amendment.

V. Summary of claimed subject matter

The present invention provides a non-volatile memory cell. The non-volatile memory cell comprises a substrate, a gate, a first source/drain region, a composite dielectric layer, a second source/drain region and a third source drain region. The substrate has a trench formed therein and the gate is located within the trench. Furthermore, the first source/drain region is

located at the bottom of the trench and the composite dielectric layer is located between the gate and the surface of the trench. The composite dielectric layer comprises at least a charge-trapping layer. The second source/drain region is located in the substrate on one side of the gate and the third source/drain region is located in the substrate on the other side of the gate. The second source/drain region and the third source/drain region are electrically connected to a common bit line.

Since the second source/drain region and the third source/drain region are electrically connected to the same common bit line, a single non-volatile memory cell can be regarded as two cells connected in parallel. That is, a first cell, which is composed of the first source/drain region, the second source/drain region and the gate, and a second cell, which is composed of the first source/drain region, the third source/drain region and the gate are connected in parallel. In this dual cell structure, the gates of the cells are electrically connected to a common word line, the sources are electrically connected to the same common source line and the drains are electrically connected to the same common bit line. That is, the adjacent cells share the same gate and the same source and the drains of the adjacent cells are connected to the same common bit line. Hence, with this configuration, the density of current flowing through the non-volatile memory cell is increased and the efficiency of programming/erasing operation is improved.

VI. Grounds of rejection to be reviewed on appeal

Were claims 1-6 and 9-10 properly rejected under 35 U.S.C. 103(a) as being obvious over Chang et al. (U.S. 6,486,028; hereafter Chang) in view of Fastow et al. (U.S. 6,583,479; hereafter Fastow)?

Were claims 7 and 8 properly rejected under 35 U.S.C. 103(a) as being obvious over Chang in view of Fastow and further in view of Forbes (U.S. pub. No. 2003/0235076; hereafter Forbes)?

VII. Arguments

A. The related law

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984). There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998). "Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." In re Kozab, 217 F.3d 1365, 1371 (Fed. Cir. 2000).

Combination claims can consist of new combination of old elements or combinations of new and old elements....Because old elements are part of these combination claims, claim limitations may, and often do, read on the prior art....It is well established in patent law that a claim may consist of all old elements, such as the rigid-conduit system, for it may be that the combination of the old elements is novel and patentable. Similarly, it is well established that a claim may consist of all old elements and one new element, thereby being patentable. *Clearstream Wastewater Sys., Inc. v. Hydro-Action, Inc.*, 206 F.3d 1440, 54 USPQ2d 1185 (Fed. Cir. 2000) (citing Intel Corp. v. United States Int'l Trade Comm'n, 946 F.2d 821, 842, 20 USPQ2d 1161, 1179 (Fed. Cir. 1991); Panduit Corp. v. Dennison Mfg., 810 F.2d 1561, 1575, 1 USPQ2d 1593, 1603 (Fed. Cir. 1987)).

Most if not all inventions arise from a combination of old elements....Thus, every element of a claimed invention may often be found in the prior art....However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *In re Kotzab*, 217 F.3d 1365, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000)

B. Grouping of the claims

For the ground of rejection contested by appellants in this appeal, claims 1-10 may be treated as one group to stand or fall together. Independent claim 1, the sole independent claim pending, may be taken as representatives for the issue on appeal.

C. *Claims 1-6 and 9-10 were improperly rejected under 35 U.S.C. 103(a) as being obvious over Chang in view of Fastow.*

1. The rejection

The Final Office Action, dated May 20th, 2005, rejected claims 1-10 under 35 USC §103(a) over Chang et al. (U.S. 6,486,028; hereafter Chang) in view of Fastow et al. (U.S. 6,583,479; hereafter Fastow). In making the rejection, the Examiner has construed Chang to disclose the non-volatile memory cell except the third source/drain region located in the substrate on the other side of the gate. The Examiner cites Fastow to teach a third source/drain region located in the substrate on the other side of the gate, wherein the second source/drain region and the third source/drain region are electrically connected to a common bit line. In response to the Final Office Action dated May 20th, 2005, a telephone interview was held with the Examiner on July 11th, 2005. During the telephone interview, the Examiner acknowledges the appellants' point that the second the third source/drain regions 214 (as shown in Fig. 2B and Fig. 3 of the invention), on each side of the gate respectively, are connected to a same bit line 220 through plugs 218 whereas the alleged second the third source/drain regions of cited reference (Fastow et al., U.S. 6,583,479) are connected to separate bit lines 826. However, an Advisory Action dated on September 13th, 2005 after the appellants filed the Final Response on August 18th, 2005 stated that "drain and sources are interchangeable. Therefore, figure 8 of Fastow shows drains 806 and 808 contact the common bit line 826".

2. The prior art

Chang discloses a nitride read-only-memory cell vertical structure. As shown in Fig. 6 of Chang's application, a gate conductive layer 116 is formed over the substrate 100 and filling the trench 102. The source/drain region 108 is located in the substrate 100 at a bottom of the trench 102, and the source/drain regions 104 and 106 are located in the substrate 100 in the upper corners of the trench 102 respectively.

Fastow discloses a two bit flash EEPROM cell. In Fig. 10 and col. 14, lines 36-38 of Fastow's application, Fastow shows that the sources of the cells 822 and 824 are connected to a contact 820 and, however, the drains of cells 822 and 824 are connected to the different contacts 826 respectively.

3. The prior art differentiated

The proposed invention is directed to a single non-volatile memory cell composed of two parallel connected cells. In a non-volatile memory cell, the parallel connected cells share the same gate and the same source (the first source/drain region) and the drains (the second and the third source/drain regions) of the parallel connected cells are electrically connected to the same common bit line (as shown in Fig. 3 and paragraph [0036]). Hence, with this configuration, the density of current flowing through the non-volatile memory cell is increased and the efficiency of programming/erasing operation is improved. What significantly distinguishes the structure of claim 1 of the proposed invention is that the second source/drain region and the third source/drain region, on each side of the gate respectively, are connected to a same bit line.

As clearly shown in the prior art Chang and admitted by the Examiner, the source/drain regions 104 and 106 are not connected to the same common bit line.

The Office Action cites Fastow for teaching that, as shown in Fig. 10 of Fastow's application, the source/drain regions 806 and 808 are connected to the same contact 826. The Examiner in the Advisory Action further stated that the source and drain are interchangeable so that the drains of different cells can connected to the same bit line as well. However, Fastow teaches differently by disclosing that the cells 822 and 824 share the source 804 but the drains 806 and 808 of the cells 822 and 824 are connected to different bit lines 826 (as shown in Fig. 9 and Fig. 10 of Fastow's application).

The Examiner's assertion that Fastow teaches the drain 806 of the cell 822 and the drain 808 of the cell 824 are connected to the same bit line 826 is totally unsubstantiated because Fastow clearly suggests that the drain 806 of the cell 822 and the drain 808 of the cell 824 are connected to different bit lines, respectively (as shown in Fig. 8 together with Fig. 10).

Even considering that the source and the drain are interchangeable, the structure disclosed by Fastow after the source interchanges with the drain of each cell is obviously different from the structure taught in the present invention. That is, in the proposed invention, the adjacent cells are sharing the same source and the drains of the adjacent cells are connected to the same bit line. Nevertheless, in the structure disclosed by Fastow after the source interchanges with the drain of each cell, the adjacent cells are sharing the same drain and the same bit line but the sources of the adjacent cells are connected to the different source lines respectively. The interconnection between the adjacent cells, after interchanging the source with the drain as what suggested by the Examiner, is still different from that of the proposed invention.

4. Even if combined Chang and Fastow

The Office Action combines Chang with Fastow to modify the structure disclosed by Chang to include the interconnection relationship between the drains at top corners of the trench 102 and the bit lines taught by Fastow. However, even if combined Chang and Fastow, the adjacent cells shares the same source but have the drains being connected to the different bit lines.

D. *Claims 7-8 were improperly rejected under 35 U.S.C. 103(a) as being obvious over Chang in view of Fastow and further in view of Forbes.*

1. The rejection

The Final Office Action, dated May 20th, 2005, rejected claims 1-10 under 35 USC §103(a) over Chang et al. (U.S. 6,486,028; hereafter Chang) in view of Fastow et al. (U.S. 6,583,479; hereafter Fastow) and further in view of Forbes (U.S. pub. No. 2003/0235076; hereafter Forbes). In making the rejection, the Examiner has construed that Change in view of Fastow discloses the proposed invention except the non-volatile memory cell further comprising spacers formed on the sidewalls of the gate. The Examiner cites that Forbes teaches the non-volatile memory cell further comprising spacers formed on the sidewalls of the gate.

2. The prior art

As discussed above, the combination of Chang and Fastow only provides a memory structure with that the drains of the adjacent cells are connected to the different bit lines. Even through the source is interchanged with the drain as suggested by the Examiner, the sources of the result structure fail to connect to the same source line while the drains are connected to the same bit line.

Forbes teaches the non-volatile memory cell further comprising spacers formed on the sidewalls of the gate but fails to teach or suggest the drains of the adjacent cells being connected to the same bit line.

3. The prior art differentiated

As discussed above, proposed invention is directed to a single non-volatile memory cell composed of two parallel connected cells. In a non-volatile memory cell, the parallel connected cells share the same gate and the same source (the first source/drain region) and the drains (the second and the third source/drain regions) of the parallel connected cells are electrically connected to the same common bit line (as shown in Fig. 3 and paragraph [0036]). Hence, with this configuration, the density of current flowing through the non-volatile memory cell is increased and the efficiency of programming/erasing operation is improved. What significantly distinguishes the structure of the proposed invention is that the second source/drain region and the third source/drain region, on each side of the gate respectively, are connected to a same bit line.

However, none of the cited arts including Chang, Fastow and Forbes suggests or teaching that the drains of the adjacent cells are connected to the same bit line while the adjacent cells share the same gate and the same source.

4. Even if combined Chang, Fastow and Forbes

As discussed above, the combination of Chang, Fastow and Forbes still fails to render the proposed invention unpatentable. Even though every elements in the structure of the proposed invention is disclosed by the cited arts and well known in the art, the combination of the cited arts still fails to show the novel interconnection relationship that the drain of the adjacent cells are connected to the same bit line while the adjacent cells share the

same gate and the same source. Therefore, Appellants respectfully submit to the Board that the teachings of Chang, Fastow and Forbes are deficient in rendering claims 7-8 unpatentable.

E. Conclusion.

As noted, none of the cited art, either alone or in combination, can render the appealed claims obvious. None of the reference Chang, Fastow and Forbes teaches the source/drain regions, at each side of the gate respectively, being connected to the same common bit line. No combination of the refcrences, Chang and Fastow even further in view of Forbes, can provide a non-volatile memory cell with a structure having two parallel connected cells as taught in the present invention.

Accordingly, Appellants believe that the rejections under 35 U.S.C.§103 are in error, and respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully Submitted,

Date : Nov. 11, 2005

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VIII. Claims appendix

CLAIMS ON APPEAL:

Claim 1. (previously presented) A non-volatile memory cell, comprising:

a substrate, having a trench thereon;

a gate, formed within the trench;

a first source/drain region, formed at a bottom of the trench;

a composite dielectric layer, formed between the gate and a surface of the trench, wherein the composite dielectric layer comprises at least a charge-trapping layer;

a second source/drain region, formed in the substrate on one side of the gate; and

a third source/drain region located in the substrate on the other side of the gate, wherein the second source/drain region and the third source/drain region are electrically connected to a common bit line.

Claim 2. (original) The non-volatile memory cell of claim 1, wherein the gate completely fills the trench.

Claim 3. (original) The non-volatile memory cell of claim 1, wherein the gate fills the trench and protrudes above the substrate surface.

Claim 4. (original) The non-volatile memory cell of claim 1, wherein the gate further laterally extend above the substrate outside the trench.

Claim 5. (original) The non-volatile memory cell of claim 1, wherein the composite dielectric layer also laterally extend above the substrate outside the trench and positioned between the gate and the substrate.

Claim 6. (original) The non-volatile memory cell of claim 1, wherein the composite dielectric layer further comprises:

a bottom oxide layer, wherein the charge-trapping layer located between the gate and the bottom oxide layer; and

a cap oxide layer, located between the gate and the charge-trapping layer.

Claim 7. (original) The non-volatile memory cell of claim 1, further comprising spacers formed on the sidewalls of the gate.

Claim 8. (original) The non-volatile memory cell of claim 7, further comprising a lightly doped region formed in the substrate underneath the spacers.

Claim 9. (original) The non-volatile memory cell of claim 1, wherein material constituting the gate comprises polysilicon.

Claim 10. (original) The non-volatile memory cell of claim 1, wherein the composite dielectric layer comprises a silicon oxide/silicon nitride/silicon oxide layer.

Claim 11-18. (canceled)